# I/V CONVERTER CIRCUIT AND D/A CONVERTER

## BACKGROUND OF THE INVENTION

1. Field of Invention

**[0001]** The present invention relates to an I/V (current/voltage) converter circuit for converting current to voltage and a D/A converter using the same.

2. Description of Related Art

**[0002]** In a conventional D/A converter (hereinafter referred to as DAC), a current generating circuit, including a plurality of currentcells, generates a total current corresponding to the value of a digital signal, which is to be converted to an analog signal. An I/V converter circuit, which is also part of the DAC, converts the total current to a voltage, so that an analog signal having a voltage corresponding to the value of the digital signal is generated.

**[0003]** In the conventional DAC, however, a MOS transistor is generally used as the current generating circuit, and thus linearity failure may occur depending on the voltage of the analog signal. Also, in order to use the analog signal output from the DAC, the voltage of the analog signal generated by the DAC must be shifted in accordance with the input/output characteristics of a subsequent-stage circuit using the analog signal.

**[0004]** In this circumstance, an I/V converter circuit and a DAC are disclosed in this application, similarly to Japanese Unexamined Patent Application Publication No. 2002-118468 (hereinafter referred to as Patent Document), in which linearity failure of an analog signal can be overcome, and the level of the voltage of the analog signal can be shifted in accordance with the input/output characteristics of the subsequent-stage circuit.

**[0005]** Fig. 4 is a circuit diagram showing the configuration of an I/V converter circuit 40, which is disclosed in the Patent Document. The I/V converter circuit 40 shown in Fig. 4 includes N-type MOS transistors (hereinafter referred to as NMOSs) 42 and 44 forming a current mirror circuit; operational amplifiers 46 and 48; a P-type MOS transistor (hereinafter referred to as PMOS) 50; and a resistor 52 of a resistance R. Also, the circuit includes a current source 54 for generating a total current Isig, which corresponds to the value of a digital signal to be converted to an analog signal Vout, and which corresponds to a current supplied from the DAC. Finally, the circuit includes a current source 56 for generating a bias current Ib.

**[0006]** In the I/V converter circuit 40 disclosed in the Patent Document, the operational amplifier 46 controls the NMOSs 42 and 44 in the current mirror circuit so that

the voltage of a node A is equal to a bias voltage Vb. Also, the operational amplifier 48 controls the PMOS 50 so that the voltage of a node B is equal to the bias voltage Vb. Further, the resistor 52 converts a current (Isig+Ib), mirrored from the NMOS 42 to the NMOS 44, to a voltage by using the bias voltage Vb as a reference voltage.

**[0007]** According to the I/V converter circuit 40 of the Patent Document, the voltage of the node A, that is, the source-drain voltage of a MOS transistor of the current source 54, can be fixed to a constant voltage. Therefore, linearity failure of the analog signal Vout can be overcome. Further, by adequately changing the bias current Ib, the bias voltage Vb, and the resistance R of the resistor 52 so as to change the output level of the analog signal Vout in accordance with the input/output characteristics of the subsequent-stage circuit, the analog signal Vout can be easily transmitted to the subsequent-stage circuit.

**[0008]** Accordingly, the analog signal Vout, which is calculated by the following equation (1), is output from the I/V converter circuit 40 according to the Patent Document:

$$Vout=R\cdot(Isig+Ib)+Vb=R\cdot Isig+R\cdot Ib+Vb. \quad (1)$$

**[0009]** Herein, R·Isig is a signal component and R·Ib+Vb is a clamp component.

**[0010]** That is, the voltage of the analog signal Vout is clamped by R·Ib+Vb, and the clamp level can be arbitrarily set by changing the values of R, Ib, and Vb. However, the amplitude of a signal component changes when the value of R is changed. Also, as described above, by dynamically changing the value of Vb, linearity failure occurs and the performance of the D/A converter deteriorates. Therefore, the clamp level is controlled by changing the value of Ib while fixing the values of R and Vb.

**[0011]** However, by decreasing Ib, impedance increases and the pass band of the circuit narrows, which is inadequate for a high-speed operation. Therefore, the value of Ib must be set at a value at or beyond a predetermined value, according to a maximum frequency of the signal. On the other hand, current consumption increases when the value of Ib increases, and thus the value of Ib needs to be minimized in order to suppress current consumption. Therefore, in the conventional I/V converter circuit 40, a unit for controlling the value of Ib must be provided in order to set Ib at an adequate value.

## SUMMARY OF THE INVENTION

**[0012]** An object of the present invention is to solve the above-described problems of the conventional art and to provide an I/V converter circuit and a D/A converter in which a wide pass band of a signal can be obtained, and current consumption can be reduced.

**[0013]** In order to achieve this goal, an I/V converter circuit, according to various exemplary embodiments of the present invention, includes a current mirror circuit having a first element connected between the ground and a first node and to which a current is supplied from an input terminal, and a second element connected between the ground and a second node, to which the current supplied to the first node is mirrored. The I/V converter also includes a first bias-current generating circuit, which supplies a first bias current to the first node and which adjusts the amount of the current supplied to the first node, and a first control circuit, which receives the voltage of the first node and a bias voltage at the input side and which controls the first and second elements of the current mirror circuit so that the voltage of the first node is substantially equal to the bias voltage. The I/V converter, according to various exemplary embodiments, also includes a second bias-current generating circuit, which supplies a second bias current to the second node and which adjusts the amount of the current supplied to the second node, a third element which is connected between the second node and an output terminal and which converts a current flowing therethrough to a voltage by using the bias voltage as a reference voltage, and a second control circuit which receives the voltage of the second node and the bias voltage at the input side and which controls the voltage output from the output terminal so that the voltage of the second node is substantially equal to the bias voltage.

**[0014]** Preferably, according to various exemplary embodiments, the second bias current is m times larger than the first bias current, and a current flowing through the second element of the current mirror circuit is m times larger than a current flowing through the first element.

**[0015]** Also, the first and second elements of the current mirror circuit may be N-type MOS transistors, the third element may be a resistor, and the first and second control circuits may be operational amplifiers.

**[0016]** The I/V converter circuit may further include a unit for changing the bias voltage.

**[0017]** A D/A converter according to various exemplary embodiments of the present invention includes a current generating circuit, for generating a total current corresponding to the value of a digital signal which is to be converted to an analog signal, and the above-described I/V converter circuit. The total current generated by the current generating circuit, according to various exemplary embodiments, is supplied from the input terminal of the I/V converter circuit to the first node.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0018]** Fig. 1 is a circuit diagram showing the configuration of an I/V converter circuit, according to various embodiments of the present invention;

**[0019]** Fig. 2 is a circuit diagram showing the configuration of an I/V converter circuit, according to various embodiments of the present invention;

**[0020]** Fig. 3 is a circuit diagram showing the configuration of current sources according to various embodiments of the present invention; and

**[0021]** Fig. 4 is a circuit diagram showing the configuration of a conventional I/V converter circuit.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0022]** Hereinafter, an I/V converter circuit and a D/A converter using the same, according to preferred embodiments of the present invention, will be described with reference to the attached drawings.

**[0023]** Fig. 1 is a circuit diagram showing the configuration of an I/V converter circuit 10 according to an embodiment of the present invention. The I/V converter circuit 10 shown in Fig. 1 serves as a current/voltage converter circuit used for the output stage of a D/A converter (hereinafter referred to as DAC) according to various exemplary embodiments of the present invention. The I/V converter includes N-type MOS transistors (hereinafter referred to as NMOSs) 12 and 14, operational amplifiers 16 and 18, an element 20, which may be a resistor, and current sources 22 and 24. Also, according to various exemplary embodiments, the circuit includes a current source 26, which represents a total current corresponding to the value of a digital signal and a load CL.

**[0024]** Herein, a common signal (output signal of the operational amplifier 16) is input to the gates of the NMOSs 12 and 14, and the NMOSs 12 and 14 form a current mirror circuit. That is, as will be described below, the same amount of current Isig+Ib1 constantly flows through the NMOSs 12 and 14. The NMOS 12 is connected between a node A and the ground, and the NMOS 14 is connected between a node B and the ground.

**[0025]** Each of the operational amplifiers 16 and 18 functions as a control circuit for adjusting the voltage of the output signal thereof so that the same voltage is input to the positive (+) terminal and the negative (-) terminal thereof. In the operational amplifier 16, a voltage Vb1 of the node A is input to the positive (+) terminal and a bias voltage Vb is input to the negative (-) terminal, and the output signal of the operation amplifier 16 is input to the gates of the NMOSs 12 and 14. In the operational amplifier 18, a voltage Vb2 of the node B

is input to the positive (+) terminal and a bias voltage Vb is input to the negative (-) terminal and the output signal of operational amplifier 18 is output as an analog signal Vout from an output terminal V.

**[0026]** Element 20, according to various exemplary embodiments, is a resistor for converting a current I flowing therethrough to a voltage V by using the voltage Vb2 of the node B as a reference voltage, and is located between the output terminal V and the node B. The resistance of element 20 is R.

**[0027]** The current source 22, according to various exemplary embodiments, serves as a current generating circuit for generating a bias current Ib1 for fine adjustments of the current amount and supplying the bias current Ib1 to the node A. The current source 22 is connected between a power supply and the node A. Likewise, according to various exemplary embodiments, the current source 24 serves as a current generating circuit for generating a bias current Ib2 for fine adjustments of the current amount and supplying the bias current Ib2 to the node B. The current source 24 is located between a power supply and the node B.

**[0028]** The current source 26 serves as a current generating circuit for generating the total current Isig corresponding to the value of a digital signal, which is to be converted to the analog signal Vout, in the DAC according to various exemplary embodiments of the present invention. The total current Isig is supplied from an input terminal I of the I/V converter circuit 10 to the node A. The DAC, according to the various exemplary embodiments of the present invention, includes this current generating circuit and the I/V converter circuit 10 shown in Fig. 1.

**[0029]** Next, the operation of the I/V converter circuit 10, according to various exemplary embodiments, will be described.

**[0030]** The total current Isig is supplied from the current source 26 to the node A through the input terminal I. The total current Isig changes in accordance with the value of a digital signal that is to be converted to the analog signal Vout by the DAC according to various exemplary embodiments of the present invention.

**[0031]** In the I/V converter circuit 10, the voltage of the output signal of the operational amplifier 16 changes so that the voltage Vb1 of the node A is constantly equal to the bias voltage Vb regardless of change in the total current Isig. The output signal of the operational amplifier 16 is input to the gate of the NMOS 12, so that the on-resistance of the NMOS 12 changes. Accordingly, the voltage Vb1 of the node A is controlled so as to be

constantly equal to the bias voltage Vb, regardless of change in the total current Isig.

**[0032]** Accordingly, in the I/V converter circuit 10, the voltage Vb1 of the node A, that is, a voltage Vds between the source and drain of a MOS transistor serving as the current source 26 for generating the total current Isig corresponding to the value of the digital signal, is controlled so as to be kept at a constant value. Accordingly, linearity failure of the DAC can be overcome.

**[0033]** The NMOSs 12 and 14 form a current mirror circuit, as described above. A current Isig+Ib1, which is created by adding the total current Isig supplied from the current source 26 and the bias current Ib1 supplied from the current source 22, flows through the NMOS 12. Therefore, as in the NMOS 12, the on-resistance of the NMOS 14 changes in accordance with the output signal of the operational amplifier 16, and the same amount of current Isig+Ib1 as in the NMOS 12 thus constantly flows through the NMOS 14.

**[0034]** Moreover, the voltage of the analog signal Vout, which is output from the output terminal V, that is, the voltage of the output signal of the operational amplifier 18, changes so that the voltage Vb2 of the node B is constantly equal to the bias voltage Vb. As described above, since a current flowing through the NMOS 14 is Isig+Ib1, a current flowing through element 20 is Isig+Ib1-Ib2. Accordingly, if Ib1 is approximately equal to ($\approx$) Ib2, then the current flowing through element 20 is Isig.

**[0035]** The current Isig flowing through element 20, according to various exemplary embodiments, is I/V converted by the resistance R, and is output as the analog signal Vout=Isig·R+Vb2. Thus, since Vb1$\approx$Vb2$\approx$Vb, the analog signal is represented by Vout=Isig·R+Vb.

**[0036]** That is, the voltage of the analog signal Vout is clamped by the voltage Vb2 of the node B, which is approximately equal to the bias voltage Vb. Therefore, by adequately setting the bias voltage Vb in accordance with the input/output characteristics of a subsequent-stage circuit which uses the analog signal Vout of the DAC, the output level of the analog signal Vout can be changed, and thus the analog signal Vout can be easily transmitted to the subsequent-stage circuit.

**[0037]** Furthermore, the voltage of the analog signal Vout does not depend on the values of the bias currents Ib1 and Ib2. Therefore, a circuit for controlling the values of the bias currents Ib1 and Ib2 is not necessary, and the circuit can be miniaturized, thus the cost can be reduced. Also, the bias currents Ib1 and Ib2 can be set at or beyond a predetermined value, according to a maximum frequency of the signal, while minimizing the bias currents

Ib1 and Ib2, so that the current consumption can be reduced. Finally, the load CL is directly driven by the operational amplifier 18. Therefore, even when the total current Isig is equal to zero (0) and no current flows through element 20, the impedance does not increase and thus the pass band is not narrowed.

**[0038]** Next, a case where the output amplification factor is changed in the I/V converter circuit 10 shown in Fig. 1, according to various exemplary embodiments, will be described.

**[0039]** Fig. 2 is a circuit diagram showing the configuration of an I/V converter circuit 30, according to various embodiments of the present invention. In the I/V converter circuit 30 shown in Fig. 2, a current source 24' and a NMOS 14' are used instead of the current source 24 and the NMOS 14 of the I/V converter circuit 10 shown in Fig. 1. A current flowing through the current source 24' and the NMOS 14' is m times larger than the current flowing through the current source 24 and the NMOS 14. Otherwise, the configuration of the I/V converter circuit 30 is the same as that of the I/V converter circuit 10, and thus the same elements are denoted by the same reference numerals and the corresponding description will be omitted.

**[0040]** Fig. 3 is a circuit diagram showing the configuration of current sources, according to various exemplary embodiments. As shown in Fig. 3, the current sources 22 and 24' are formed by using P-type MOS transistors (hereinafter referred to as PMOSs) 32 and 34. The PMOS 32 is connected between the power supply and node A and the PMOS 34 is connected between the power supply and node B. Furthermore, a signal Vgate is input to the gates of the PMOSs 32 and 34, so that a current mirror circuit is formed.

**[0041]** Accordingly, the transistor size of the PMOS 34 is m times larger than the transistor size of the PMOS 32. Therefore, when a bias current generated by the current source 22 is Ib, a bias current generated by the current source 24' is m . Ib.

**[0042]** Likewise, the transistor size of the NMOS 14' constituting the current mirror circuit is m times larger than that of the NMOS 12. Therefore, since a current flowing through the NMOS 12 is Isig+Ib, a current flowing through the NMOS 14' is m.(Isig+Ib).

**[0043]** Accordingly, the analog signal Vout output from the output terminal V can be represented by the following equation (2):

$$Vout=\{m.(Isig+Ib)-m.Ib\}\cdot R+Vb2=m\cdot Isig\cdot R+Vb. \quad (2)$$

**[0044]** As can be understood from this equation, the analog signal Vout does not depend on the bias current Ib at all, even when the output amplification factor is increased m

times.

**[0045]** In the exemplary embodiments shown in Figs. 1 and 2, the I/V converter circuit is realized by using NMOSs 12 and 14 (14') as current mirror circuits and the operational amplifiers 16 and 18 as control circuits. However, the present invention is not limited to this configuration, and the I/V converter circuit according to the present invention may be formed by using another configuration for realizing the same function. Preferably, a unit for setting the bias voltage Vb may be provided so that the bias voltage Vb can be changed in accordance with the input/output characteristics of the subsequent-stage circuit.

**[0046]** The DAC according to the present invention uses the I/V converter circuit according to the present invention, examples of which are shown in Figs. 1 and 2, as the output stage of the current generating circuit. Any type of current generating circuit may be used as long as it generates a total current corresponding to the value of a digital signal which should be converted to an analog signal, and any conventional current generating circuit may be used.

**[0047]** However, the present invention is not limited to the above-described exemplary embodiments, and various improvements and modifications may be performed without deviating from the scope of the present invention.

**[0048]** According to various exemplary embodiments of the present invention, linearity failure in the DAC can be overcome, and the output level of the analog signal can be changed in accordance with the input/output characteristics of the subsequent-stage circuit. Furthermore, since the voltage of the analog signal Vout does not depend on the value of the bias current, a circuit for controlling the value of the bias current is not necessary. Accordingly, the circuit can be miniaturized and the cost can be reduced. Also, since the bias current can be set at or beyond a predetermined value in accordance with the maximum frequency of the signal, while at the same time minimizing it, current consumption can be reduced. Finally, since the load is directly driven by the operational amplifier 18, which serves as a second control circuit, the pass band of the analog signal is not narrowed even when no current flows through the resistor.